Co-sputtered Amorphous Nb_xSi_{1-x} Barriers for Josephson-Junction Circuits

Burm Baek, Paul D. Dresselhaus, and Samuel P. Benz

Abstract— **Co-sputtered amorphous Nb_xSi_{1-x} has been developed as a barrier material for Josephson junction array circuits. This material is not only promising as a normal-metal barrier for state-of-the-art Josephson voltage standards, but the capability of tuning the barrier resistivity over a wide range (including the metal-insulator transition) could lead to applications in high-speed superconductive electronics. The electrical characteristics and uniformity of amorphous Nb_xSi_{1-x}-barrier junctions are similar to those of other normal-metal barriers, but the superior etching properties makes this barrier material especially promising for tall, stacked junctions that are required for high-junction-density applications. Under appropriate deposition conditions, the reproducibility of devices with co-sputtered amorphous Nb_xSi_{1-x} is sufficient to produce high-quality stacked-junction superconductive devices.**

Index Terms—**Amorphous alloy, Josephson arrays, metal-insulator transition, superconducting devices, thin film devices.**

I. Introduction

JOSEPHSON junctions with normal-metal barriers have become the predominant devices for dc programmable and ac Josephson voltage standards [1]-[4]. Their main advantage is that the intrinsic shunt of these superconductor-normal metal-superconductor (SNS) junctions makes them nonhysteretic, whereas superconductor-insulator-superconductor (SIS) junctions require external shunt resistors, which are a large drawback for complex designs. However, SNS Josephson junctions have a relatively lower characteristic voltage than SIS junctions due to the low resistivity of the normal-metal barrier. For internally-shunted, high-speed applications, superconductor-insulator-normal metal-insulator-superconductor (SINIS) junctions have also been successfully demonstrated [5]. There has also been research to make high-speed, nonhysteretic junctions with high-resistance barriers using reactive sputtering deposition [6] or a thickening of the Al in the standard SIS process [7], but reproducible electrical properties have not yet been shown for these junctions.

On the other hand, co-sputtering metal and silicon is another way to tune deposited thin film properties [8]. Compared to other methods and materials, the electrical properties of these amorphous films are much easier to control: adjusting the relative sputtering rate determines the stoichiometry and thus the resistivity, and the barrier thickness for a given stoichiometry determines the characteristic voltage [9]. The sputtering rates are controlled by the sputter gun power, which is reliably controlled with a commercial power supply.

Amorphous metal silicide barriers also have advantageous material properties. Their etching properties are similar to those of Nb, which is used for the superconducting electrodes. Also, because amorphous Nb_xSi_{1-x} is a disordered metal (at Nb content greater than the metal-insulator transition) the resistivity can be both large and uniform throughout the film. Amorphous Nb_xSi_{1-x} alloys with various compositions have been investigated by Hertel *et al*. [8] and Josephson junctions using them as barriers have been studied by Barrera and Beasley [9]. At Nb concentrations above 18 %, Nb_xSi_{1-x} has a finite superconducting transition temperature T_c. At concentrations below ~18 %, the resistivity becomes higher and the material passes through the metal-insulator transition at ~11 % [8].

Previous work at NIST has investigated a number of metal silicide barriers and taken advantage of their etch-compatibility with Nb to produce stacked junction arrays for programmable and ac Josephson applications [10]-[13]. In particular, arrays of stacks with up to ten junctions per stack have been demonstrated with $MoSi_2$-barriers [14]. In this paper we report our research on co-sputtered Nb_xSi_{1-x} barriers to (1) improve the profile uniformity of tall stacks by more closely matching the barrier etch rate with that of Nb, and (2) improve the tuning of the junction electrical properties by controlling the stoichiometry, such that high-speed and low-speed junctions can be fabricated with the same technology.

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II. Experiments and Results

A. Amorphous NbSi Thin Films

Nb and Si were deposited in our multitarget sputtering system that was modified for co-sputtering by adding a second dc power supply, so that two guns could be powered simultaneously. The sputter guns are angled to face the substrate platen, which is rotated during deposition to improve the uniformity of the films. Films were deposited on oxidized 76 mm diameter Si wafer substrates. The substrate platen was cooled to near room temperature with flowing nitrogen gas. First we determined the argon sputter-gas pressure (4 mTorr) that produced stable films having a slightly compressive stress and a minimum slope in the resistivity *vs.* pressure relationship. Co-sputtered films were deposited with the Si sputtering power fixed at 500 W while the Nb sputtering power was varied between 38 W and 144 W. From the relative deposition rates, we calculate that the nominal Nb atomic content ranged from 9 % to 27 %. The deposition is computer-controlled, using independent shutters on each sputter gun and pre-sputtering of the targets, so that co-sputtered films are readily fabricated and highly reproducible.

Figure 1(a) shows the room-temperature resistivity of amorphous Nb_xSi_{1-x}, as a function of the Nb sputtering power. We also measured resistivity *vs.* temperature down to 4 K, as shown in Fig. 1(b) for various Nb concentrations. From the conductivity curves plotted in the inset, we infer that our accessible resistivity range includes the metal-insulator transition, previously shown to occur at ~11.5 % Nb [8]. That is, the extrapolation of the two highest resistivity curves in Fig. 1(b) implies an insulating phase at 0 K. Superconducting transition temperatures (T_c) were also measured as annotated in Fig. 1(a). Because even a moderate T_c can cause a steep temperature dependence of the junction critical current, it is optimal to keep T_c as low as possible [13]. We conclude that a power ratio between 38/500 and 72/500 for the Nb to Si gun is optimal for these investigations. A ratio higher than 72/500 results in too high a T_c, and power lower than 38 W does not yield reproducible films. However, this narrow range in Nb concentration yields a large range in barrier resistivity (between 0.7 and 6 mΩ·cm).

Another important motivation for the use of amorphous Nb_xSi_{1-x} alloy barrier is that the etch chemistry is similar to that of Nb. This is important for vertical and uniform etching for the fabrication of tall junction stacks. We determined that the etch rate for amorphous Nb_xSi_{1-x} is only ~20 % lower than the Nb etch rate. In contrast, the fastest reactive ion etching rate for $MoSi_2$, using a mixture of SF_6 and C_4F_8, was one-tenth that of Nb [14]. Because of this increased etch rate for Nb_xSi_{1-x} we were optimistic that uniformity of stacked junctions would improve compared to those with $MoSi_2$ barriers.

B. Josephson Junctions

We fabricated Josephson junction arrays and measured their electrical characteristics while varying the Nb content and barrier thickness of the amorphous Nb_xSi_{1-x} barrier. Circuit design and fabrication processes are the same as our ac and programmable Josephson voltage standards using Nb superconducting electrodes and $MoSi_2$ barriers [10], [11], [15]. The junction size is 4 μm × 8 μm, and there are 1280 stacks per series array. The junction array is embedded in the inner conductor of a coplanar transmission line to which a continuous microwave signal is applied and terminated with a 50 Ω resistor. Two superconducting bias taps are used for low-speed four-point measurements of the array, and each tap contains multiple-coil filters to prevent microwave leakage [15].

In Fig. 2, we show *I-V* curves measured with and without 12 GHz microwave power at 4 K. The inset shows a large, flat constant-voltage step, indicating good critical current uniformity throughout the array. The barrier for these devices was deposited with 72/500 ratio of sputtering power and total barrier thickness of 35 nm. These voltage steps show similar size and uniformity to the $MoSi_2$-barrier devices that are the current technology of choice at NIST.

The critical current density, J_c is plotted for various barrier resistivities and thicknesses in Fig. 3. Assuming an exponential dependence of J_c on the barrier thickness d, we can use the data from Fig. 3 to estimate the normal metal characteristic length ξ_n in $J_c = J_{c0}exp(-d/\xi_n)$ for different barrier resistivities [16-17]. We obtained ξ_n = 5.0 nm and 1.4 nm for the films with room-temperature resistivities 0.73 mΩ·cm and 6.6 mΩ·cm, respectively. As expected, the normal metal coherence length decreases as the resistivity increases. The 4 K resistivity of amorphous Nb_xSi_{1-x} tends to become very large (> 100 mΩ·cm) when the room temperature resistivity is larger than ~4 mΩ·cm, although it should be noted that as yet we have not grown films with room temperature resistivity between 0.73 mΩ·cm and 4 mΩ·cm. In order to further study the metal-insulator transition in this system, more films must be fabricated and studied in this range.

For the high resistivity barriers, the resulting normal metal resistance R_n and characteristic voltage $V_c = I_cR_n$ (where I_c is the critical current) are large, which raises the characteristic frequency ($2eV_c/h$) and the operating speed. For example, a 4 μm × 4 μm single Josephson junction having a 12-nm-thick barrier with 6.6 mΩ·cm room-temperature resistivity has V_c ~ 150 μV and a nonhysteretic *I-V* curve. When 74 GHz microwave bias is applied, the junction shows clear Shapiro steps as shown in Fig. 4. Moreover, the temperature dependence of the critical current is weaker than that found for SNS junctions with other barrier materials and constant resistivity (see Fig. 5) [13]. This weak $I_c(T)$ dependence results from the steep decrease of barrier resistivity with increasing temperature compensating the exponential decrease of the coherence length. This high-resistivity regime could be useful for high-speed superconductive electronics applications, such as single-flux quantum logic, because the junctions are fast and there is no need for external shunt resistors, which is one of the limiting factors for high-density integrated circuits. However, the extreme sensitivity of electrical parameters in this regime, namely the resistivity, to fabrication conditions requires tight thickness and

stoichiometry control to ensure adequate uniformity. These high-characteristic-voltage, high-speed junctions demand proper theoretical investigation beyond the conventional dirty-metal proximity-junction theory [18], [19].

C. Stacked Junctions

A common challenge for tunable-barrier Josephson junctions is uniformity and reproducibility. In addition, for stacked junctions the barrier must be the same for each barrier that is consecutively grown in a multi-junction stack. The co-sputtered amorphous Nb_xSi_{1-x} barriers have good uniformity for single-barrier, non-stacked arrays as shown by the *I-V* curves of Fig. 2. Fabrication is straightforward, with no special materials considerations for the barrier. The resistivity and deposition rates are reproducible from run to run and practically linear with Nb sputter power, as shown in Fig. 1(a) for the resistivity.

While the single barrier run-to-run reproducibility is good, the deposition of multiple barriers proved inconsistent, leading to non-uniform stacks with different current densities and I_cR_n products for different barriers within the stack. For example, while fabricating double-junction Nb_xSi_{1-x}-barrier stacks similar to previously fabricated $MoSi_2$-barrier stacks [10-11], measurements showed that the two barriers produced critical currents that differed by ~15 % as shown in Fig. 6(a). This same fraction of I_c difference was maintained on junctions with a wide range of dimensions, implying that a sloped, non-vertical etch was not the culprit, as that would give a percentage of I_c difference proportional to the circumference; the problem was that the barriers were not identical.

To investigate each barrier deposition step independently, we separately deposited only the bottom or top barriers on a substrate by keeping the substrate shutter closed during all other deposition steps. Measurements of resistivity and thickness on these test films indicated that the Si deposition rate was higher during deposition of the second barrier. From extensive experiments on the time dependence of the sputter rates of both sputter guns, the problem was found to be heating of the Si sputter gun, which resulted in an increase in the sputtering rate and consequently top, second-barrier junctions with lower J_c and thus lower I_c.

In order to reduce this gun-heating effect, we made a number of improvements. First we chose a conducting p-doped Si target with a Cu backing plate for better cooling of the target. We also reduced the respective sputtering power for both materials to 350 W for Si and 48 W for Nb and added pre-cooling delays before each barrier deposition step. The resulting devices with this improved process yield more uniform double-stacked arrays. Specifically we reduced the difference in critical currents from bottom to top junction to ~3 %, as shown in Fig. 6(b). This difference is comparable to our best results in $MoSi_2$-barrier devices.

III. Conclusion

We have fabricated co-sputtered amorphous Nb_xSi_{1-x} alloy-barrier Josephson junctions for superconductive integrated circuits. The film resistivities are reliably controlled by controlling the deposition sputter rates using the sputter gun power. The compatibility of this barrier with dry-etching and the similar etch-rate with Nb are especially promising for tall SNS stacked-junction arrays for high-density Josephson voltage standards. Reliable tuning of the barrier resistivity for compositions near the metal-insulator transition may be advantageous as intrinsically shunted junctions for high-speed superconducting circuit applications. We also showed that Josephson voltage standard circuits with amorphous Nb_xSi_{1-x}–barrier junctions have good uniformity and that the constant-voltage steps of arrays under microwave bias have useful current margins. Fabrication of stacked junctions revealed that the reproducibility of consecutively stacked barriers can be degraded by gun heating. Nevertheless, we were able to improve the reproducibility by making minor modifications to the co-sputtering deposition process.

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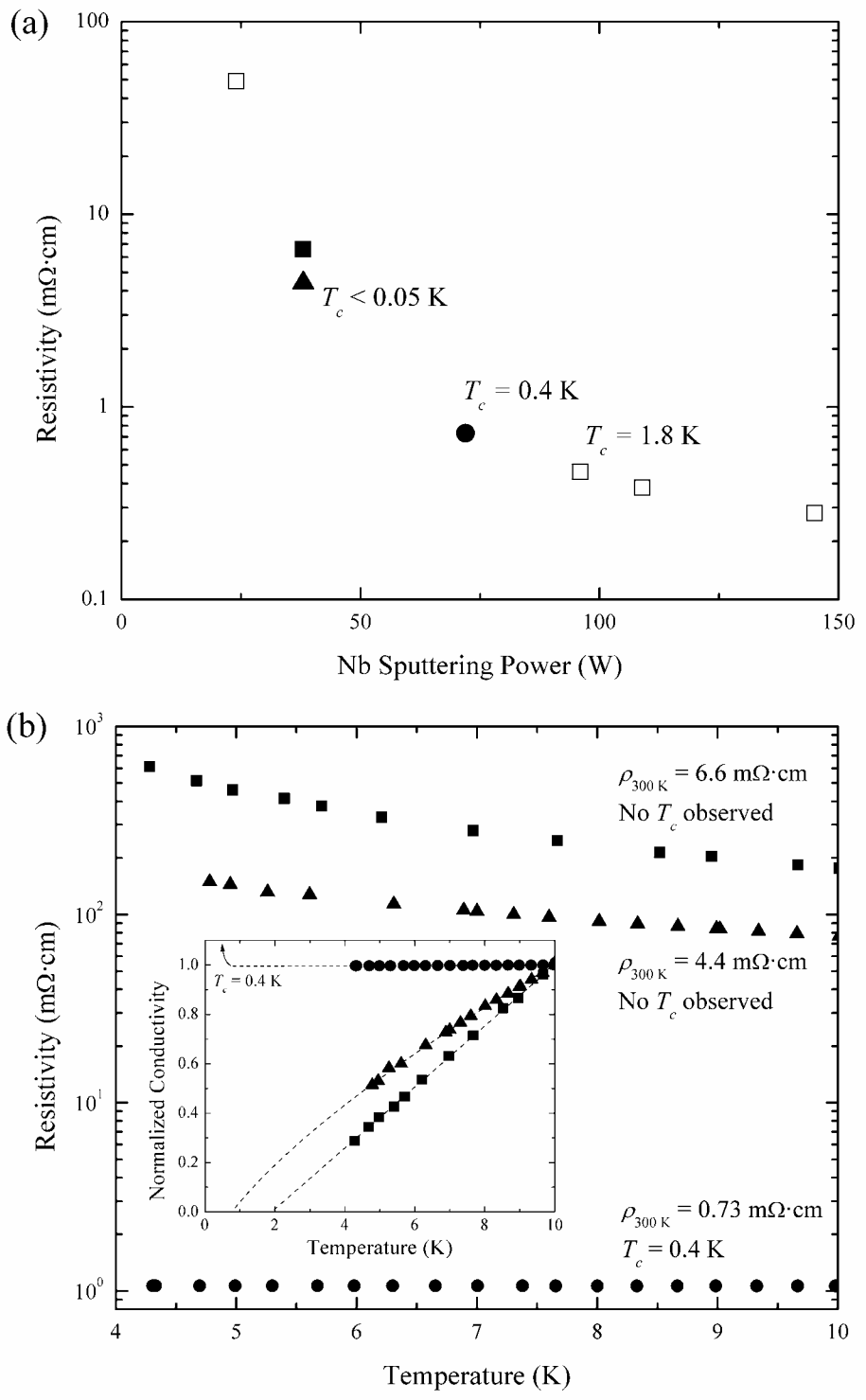

Fig. 1. Electrical properties of Nb_xSi_{1-x} thin films: (a) Room temperature resistivity as a function of Nb sputtering power and (b) temperature dependence of the resistivities for three different compositions. Inset of (b) shows the same experimental data in terms of conductivities to indicate that high resistivity films extrapolate to zero conductivity. The data are extrapolated by a power law, $\sigma(T) = \sigma_0 + \alpha T^N$ [8]. The symbols in (b) are consistent with the compositions with the same symbols in (a). The numbers around the symbols in (a) represent the measured T_c (if observed).

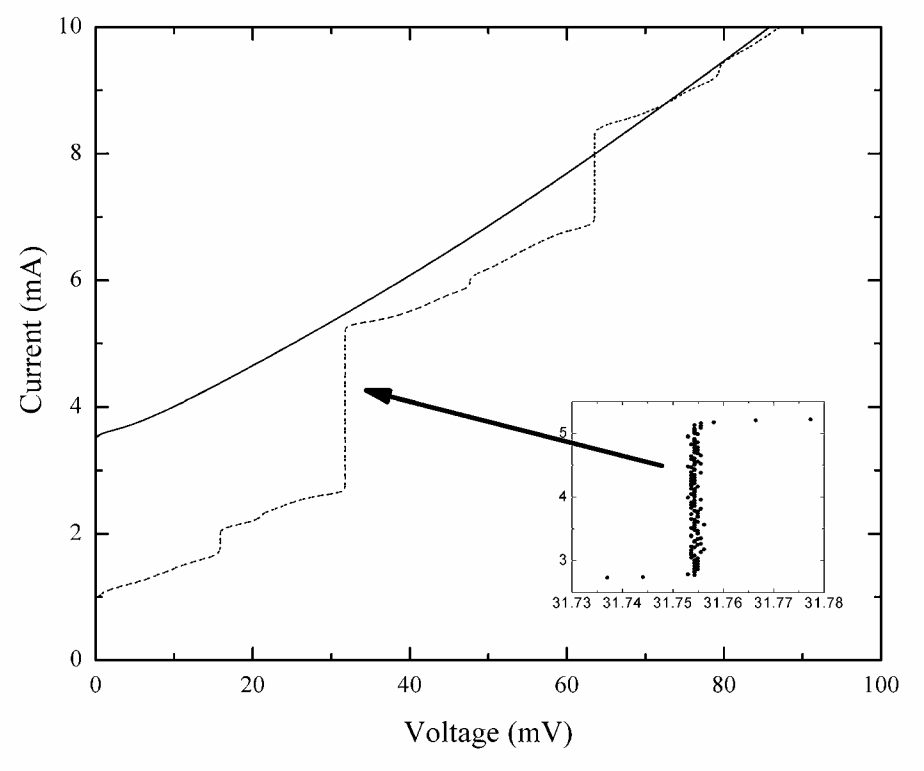

Fig. 2. Electrical characteristics of non-stacked, Nb_xSi_{1-x}-barrier Josephson junction arrays with 1280 junctions per array: (a) current-voltage curves with (dotted line) and without (solid line) a 12 GHz applied microwave bias. Each junction size is 4 μm × 8 μm. The size and flatness of the constant-voltage steps (see inset) is a qualitative measure of the array uniformity.

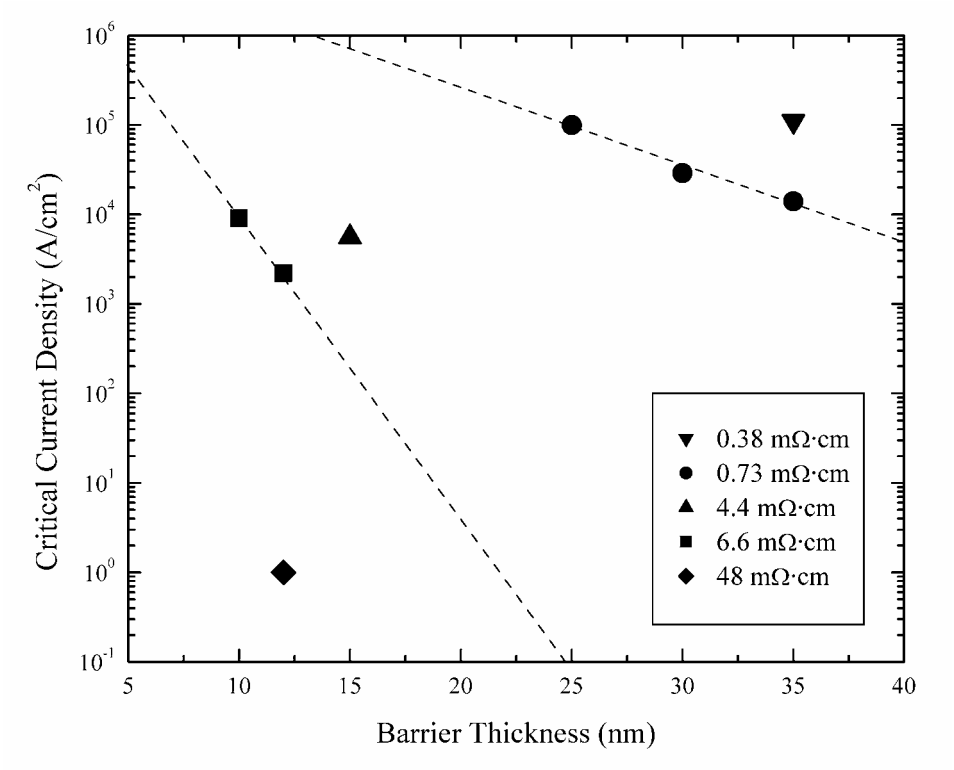

Fig. 3. Junction critical current densities at 4 K vs. barrier thickness for different (room temperature) barrier resistivities. Barrier thicknesses are nominal values calculated from (deposition rate) × (deposition time). Barrier resistivities are also nominal in the sense that the measured values are from separate films with the same deposition conditions as the corresponding barriers for Josephson junctions except the deposition times (5 minutes).

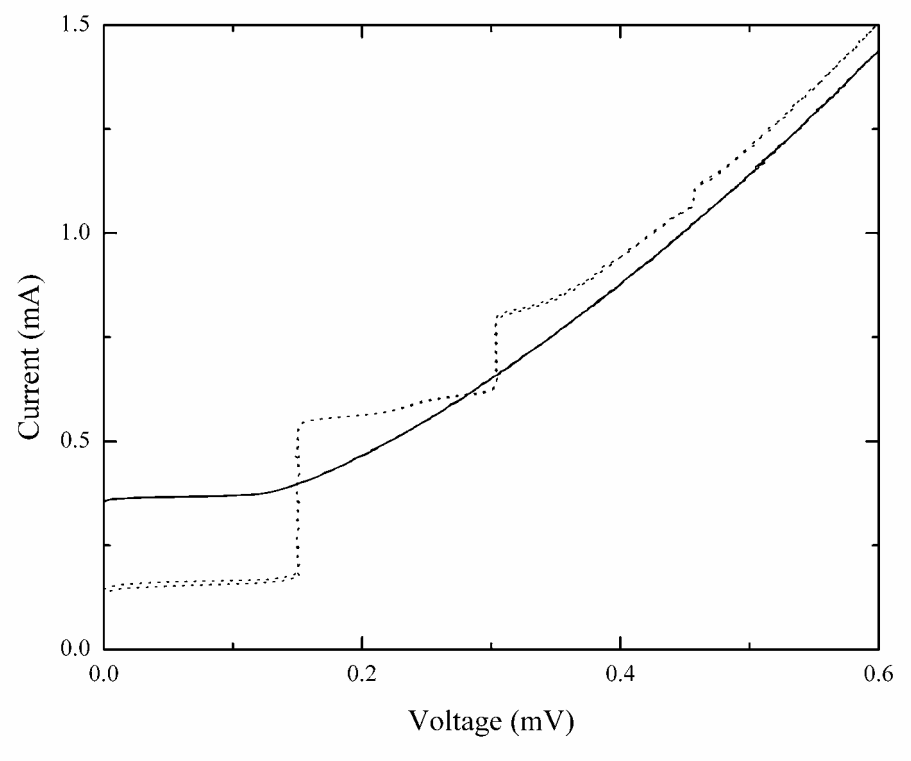

Fig. 4. Current-voltage curve of a single Josephson junction with a high-resistivity (6.6 mΩ·cm at room temperature) NbSi barrier: (solid line) without microwave irradiation and (dotted line) with 74 GHz microwave irradiation. The design size of the junction is 4.5 μm × 4.5 μm.

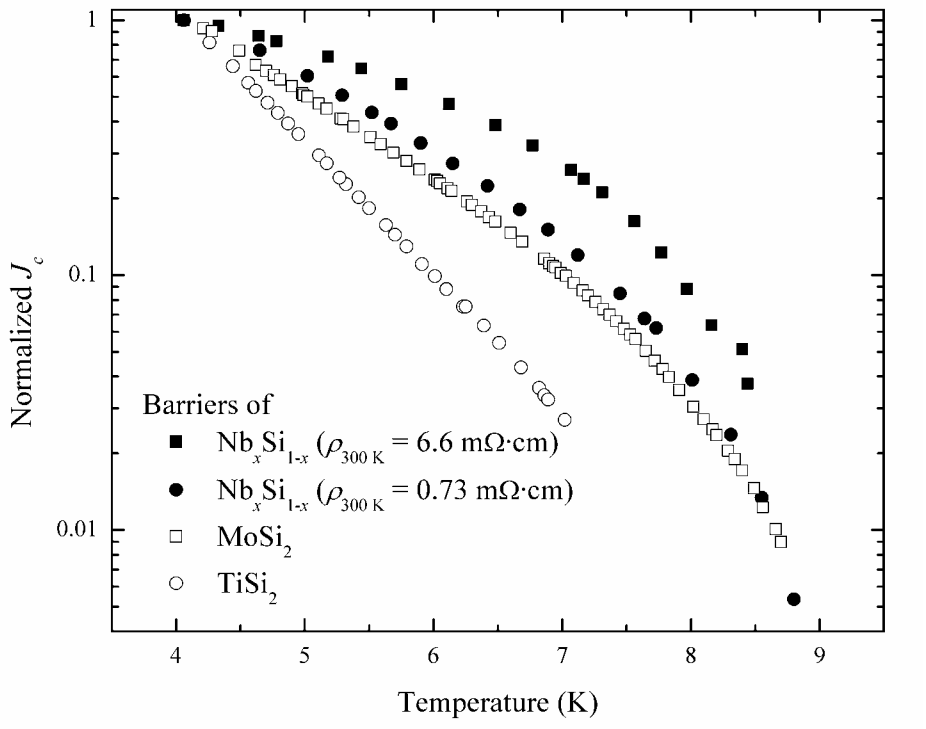

Fig. 5. Temperature dependence of the critical current density (J_c) for two kinds of co-sputtered Nb_xSi_{1-x} barriers and other metal silicide barriers. Each data set was normalized to the value of J_c at 4 K. The cases of $MoSi_2$, $TiSi_2$ and Nb_xSi_{1-x} of 0.73 mΩ·cm are well explained by conventional dirty metal SNS Josephson junction theory [12], [13], whereas that of Nb_xSi_{1-x} of 6.6 mΩ·cm has a weaker suppression of critical current density due to the steep decrease of its resistivity with increasing temperature.

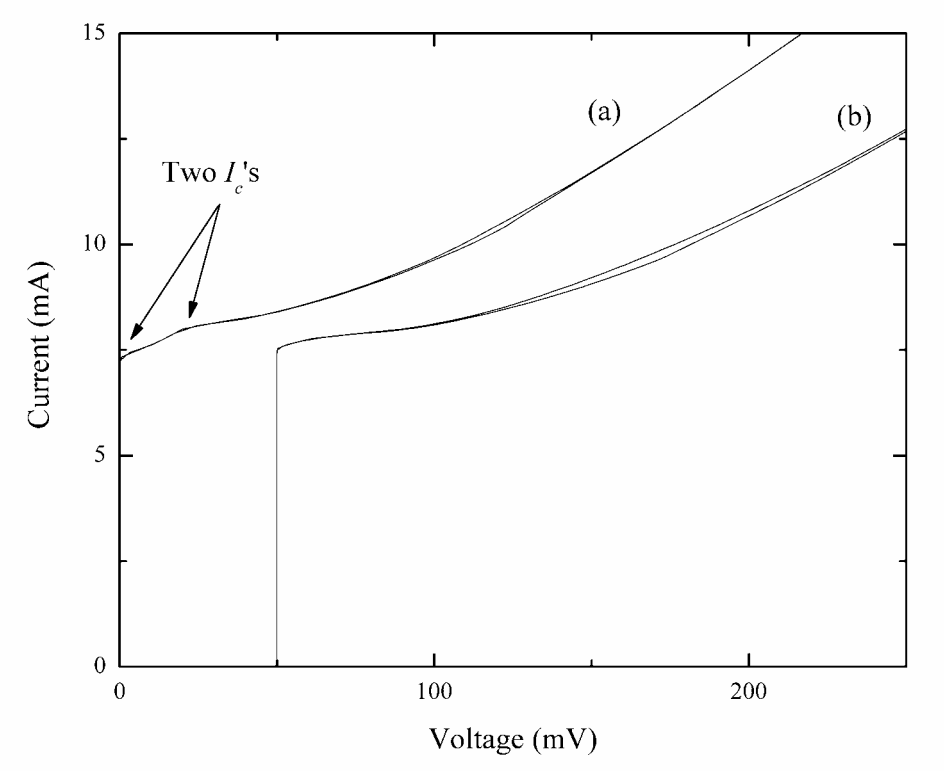

Fig. 6. Current-voltage curve at 4 K of double-stacked Josephson arrays (1280 stacks) for barriers made (a) before and (b) after improving the target heating problems ((b) is offset by 50 mV for clarity). Each junction size is 4 μm × 8 μm. In (a) an undoped Si target was sputtered at a power of 500 W with the Nb sputtering power at 72 W. The two different junctions in each stack apparently have different thicknesses, as suggested by the second critical current. In (b) the modified deposition process used a p-doped Si target with a bonded Cu backing plate, 350 W (Si) and 48 W (Nb) sputtering powers, and precooling steps before barrier depositions. At high current, the branches appear slightly hysteretic, presumably due to heating.